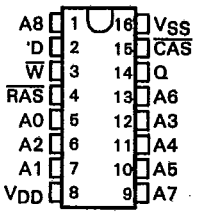
- 262,144 × 1 Organization
- Single 5-V Power Supply
  - 5% Tolerance Required for TMS4256-8
  - 10% Tolerance Required for TMS4256-10, -12, -15, and TMS4257-10, -12, -15
- JEDEC Standardized Pinouts
- Performance Ranges:

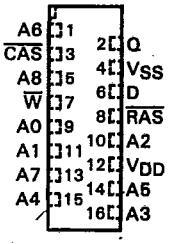
DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	V_{DD} TOLERANCE
'4256-8	80 ns	40 ns	160 ns	± 5%
'4256-10 '4257-10	100 ns	50 ns	200 ns	±10%
'4256-12 '4257-12	120 ns	60 ns	220 ns	±10%
'4256-15 '4257-15	150 ns	75 ns	260 ns	±10%

- Long Refresh Period . . . 4 ms (Max)
- Operations of the TMS4256/TMS4257 Can Be Controlled by TI's SN74ALS2967, SN74ALS2968, and THCT4502 Dynamic RAM Controllers
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Common I/O Capability with "Early Write" Feature
- Page Mode ('4256) or Nibble-Mode ('4257)
- Low Power Dissipation
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges (SMJ4256, with 10% Power Supply)

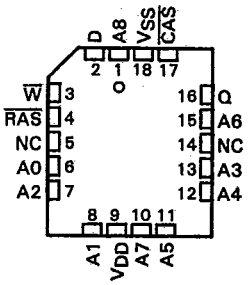
N PACKAGE
(TOP VIEW)



SD PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4256 and TMS4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The '4256-8 with a 5% voltage tolerance has a maximum $\overline{RAS}$ access time of 80 ns. The '4256/'4257-10, -12, and -15 with 10% voltage tolerances have maximum $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns, respectively.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1 V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The '4256 and '4257 are offered in 16-pin plastic dual-in-line, 16-pin plastic zig-zag in-line (ZIP), and 18-lead plastic chip carrier packages. They are guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

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refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

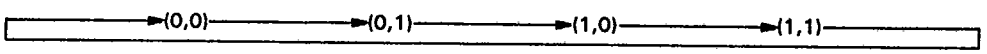
Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The external address is also ignored during the hidden refresh cycles. The data at the output pin remains valid up to the maximum $\overline{CAS}$ low pulse duration, $t_{W(CL)}$.

page mode (TMS4256)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{W(RL)}$, the maximum $\overline{RAS}$ low pulse duration.

nibble mode (TMS4257)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:

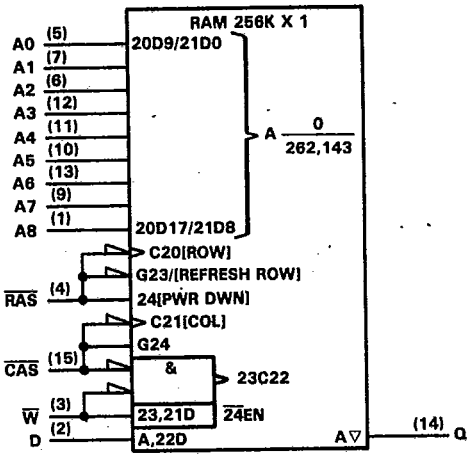


In nibble-mode, all normal memory operations (read, write, or read-modify-write) may be performed in any desired combination.

power-up

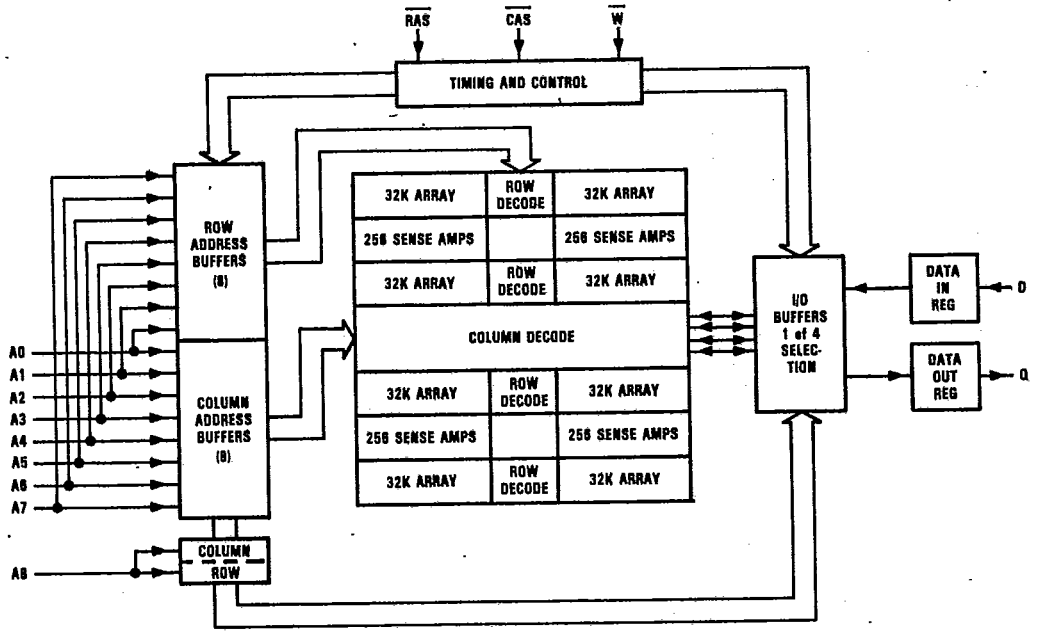
To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1084 and IEC Publication 617-12.
The pin numbers shown are for the 16-pin dual-in-line package.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin, including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage ('4256/'4257-10, -12, -15)	4.5	5	5.5	V
V_{DD}	Supply voltage ('4256-8)	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		70		70	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		4.5		4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		70		58	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		60		50	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open				45	mA

PARAMETER		TEST CONDITIONS	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		65		60	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		4.5		4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		53		48	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		45		40	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		40		35	mA

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	5	pF
$C_{i(D)}$	Input capacitance, data input	5	pF
$C_{i(RC)}$	Input capacitance strobe inputs	5	pF
$C_{i(W)}$	Input capacitance, write enable input	7	pF
C_o	Output capacitance	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		40		50	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		80		100	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	20	0	30	ns

	PARAMETER	TEST CONDITIONS	ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	30	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	70		100		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	95		135		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	160		200		ns
$t_{c(W)}$	Write cycle time	t_{WC}	160		200		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	185		235		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	20		40		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	40	10,000	50	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	70		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	80	10,000	100	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	20		30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	20		30		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	20		30		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	15		15		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	55		65		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	60		80		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		30		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	20		30		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	65		80		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

PARAMETER		ALT. SYMBOL	TMS4256-8		TMS4256-10 TMS4257-10		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	80		100		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	40		50		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	20		20		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	10		10		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		50		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	40	25	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	80		100		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

PARAMETER		ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	120		145		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	160		190		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		305		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		60		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	75	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	35		45		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	35		45		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		25		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	30		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		120		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		45		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	30		45		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		120		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

PARAMETER		ALT. SYMBOL	TMS4256-12 TMS4257-12		TMS4256-15 TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		75		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		30		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	10		20		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		70		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	25	75	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		145		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range

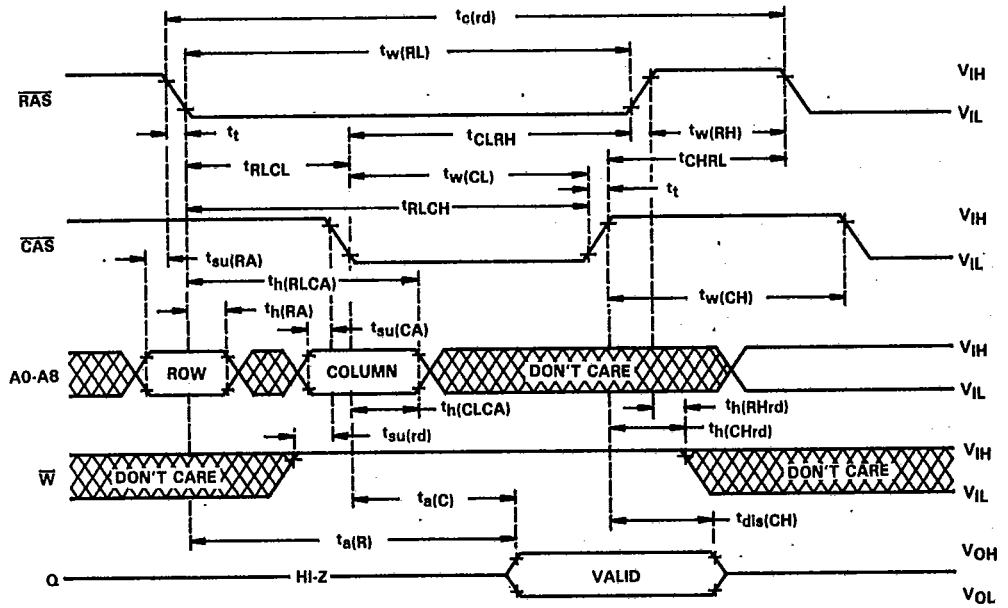
PARAMETER		ALT. SYMBOL	TMS4257-10		TMS4257-12		TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access from $\overline{CAS}$	t_{NCAC}		25		30		40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4257-10		TMS4257-12		TMS4257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	50		60		75		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	70		85		105		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	25		30		40		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	20		25		30		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	25		30		40		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	15		20		25		
$t_{su(WCHN)}$	Nibble-mode write command setup before $\overline{CAS}$ high	t_{NGWL}	20		25		35		

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

read cycle timing



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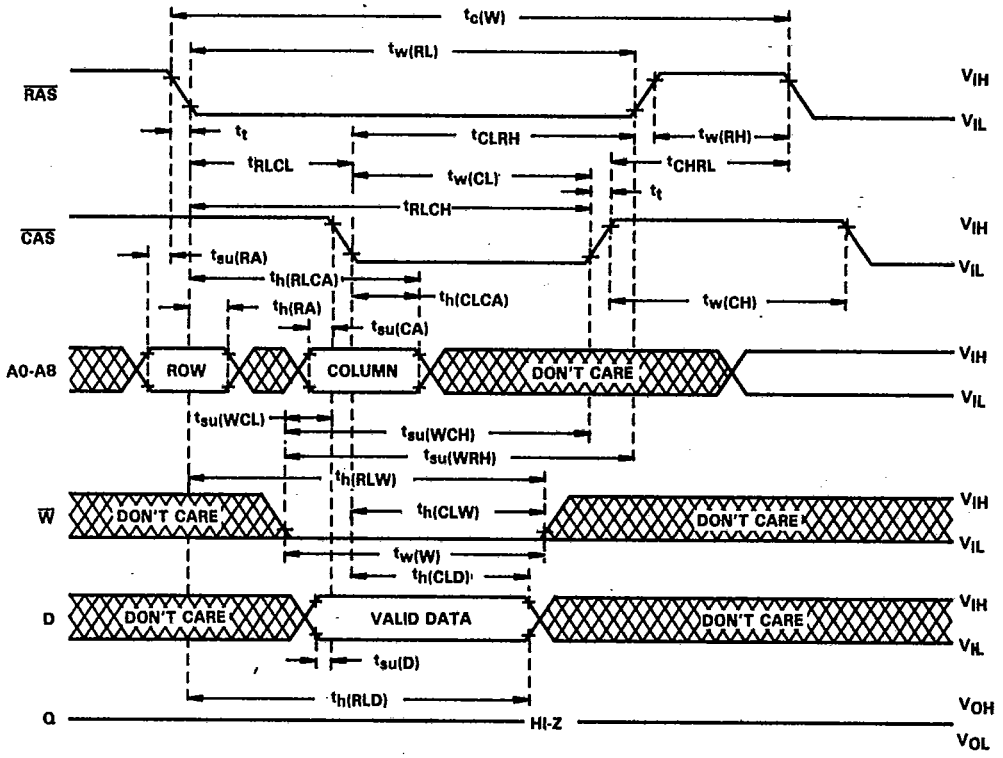
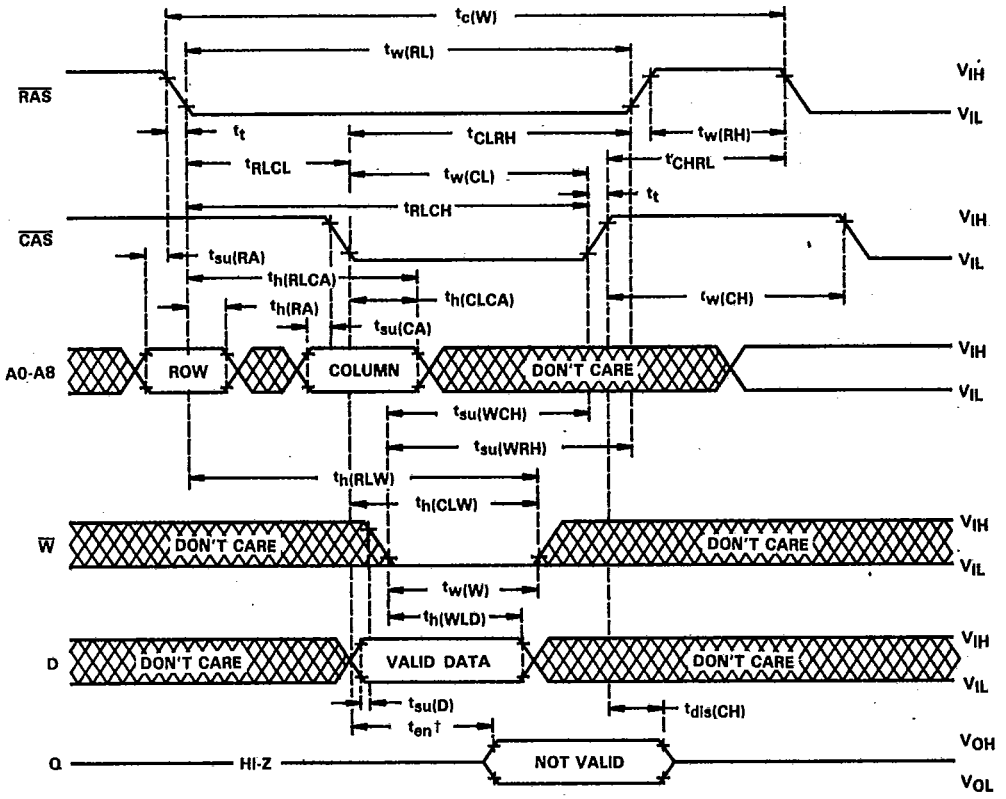
early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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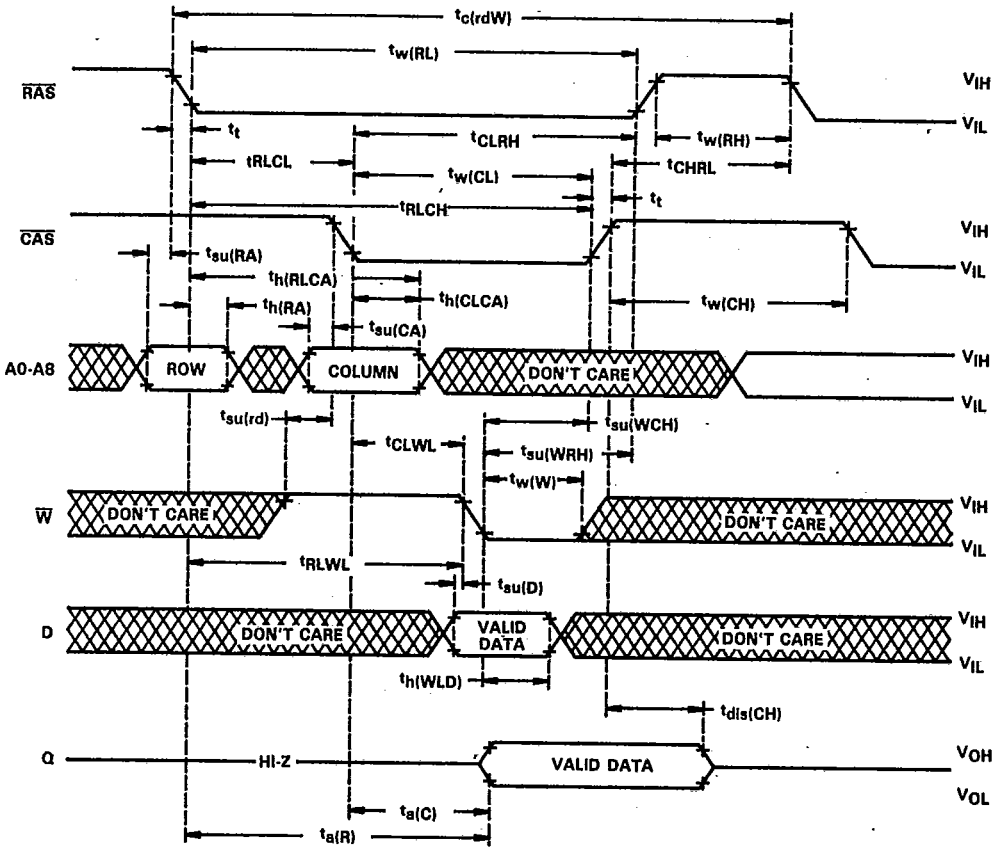
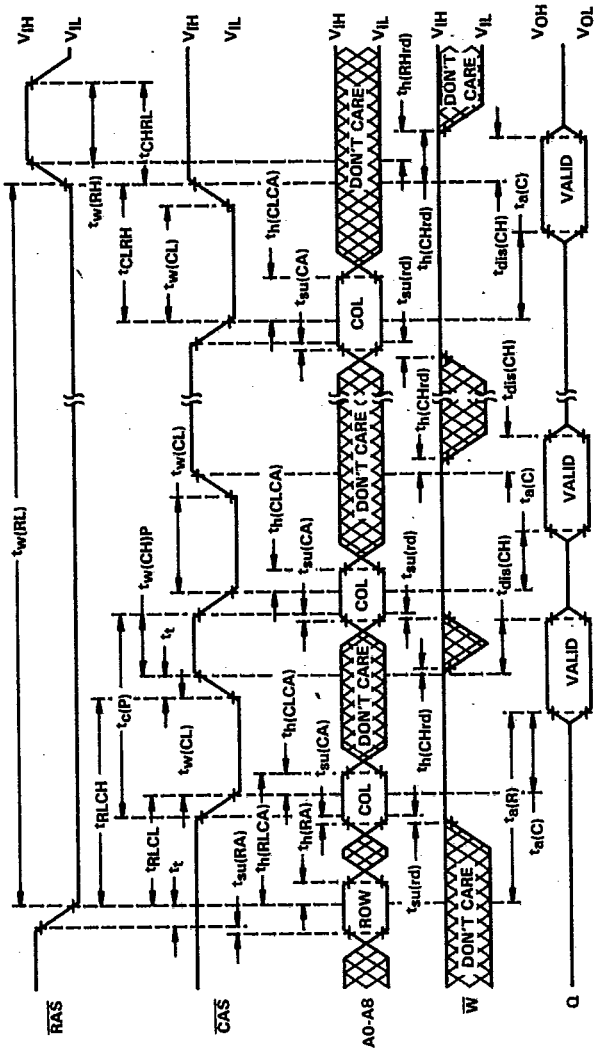
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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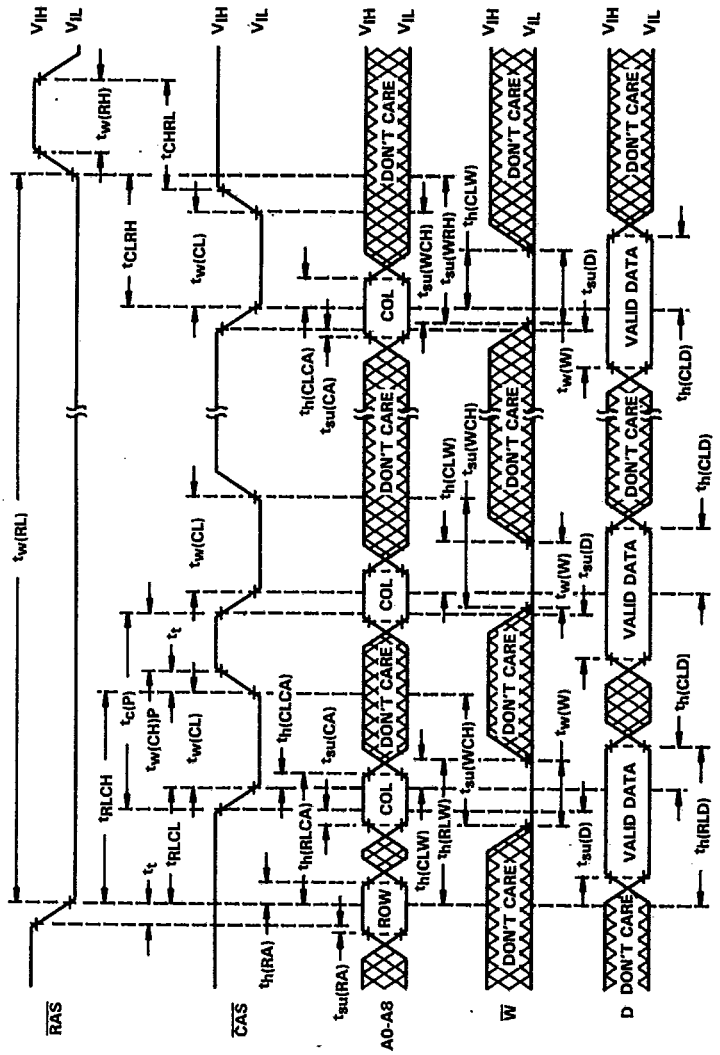
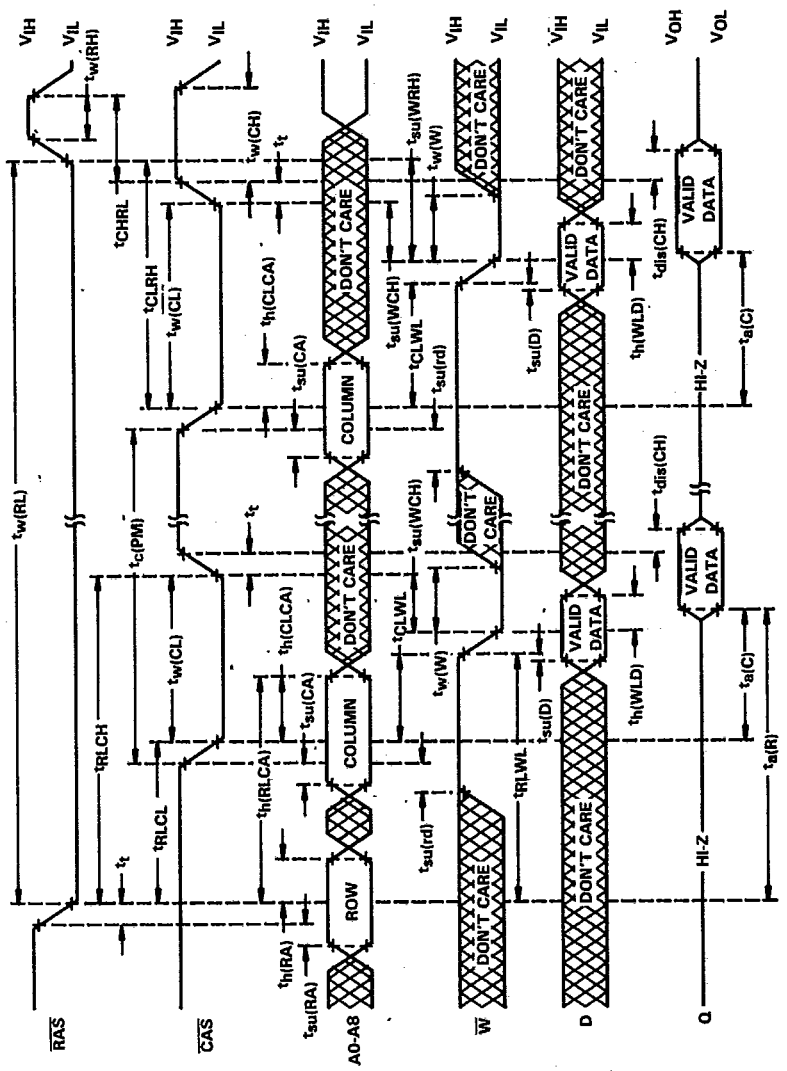
page-mode write cycle timing



NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

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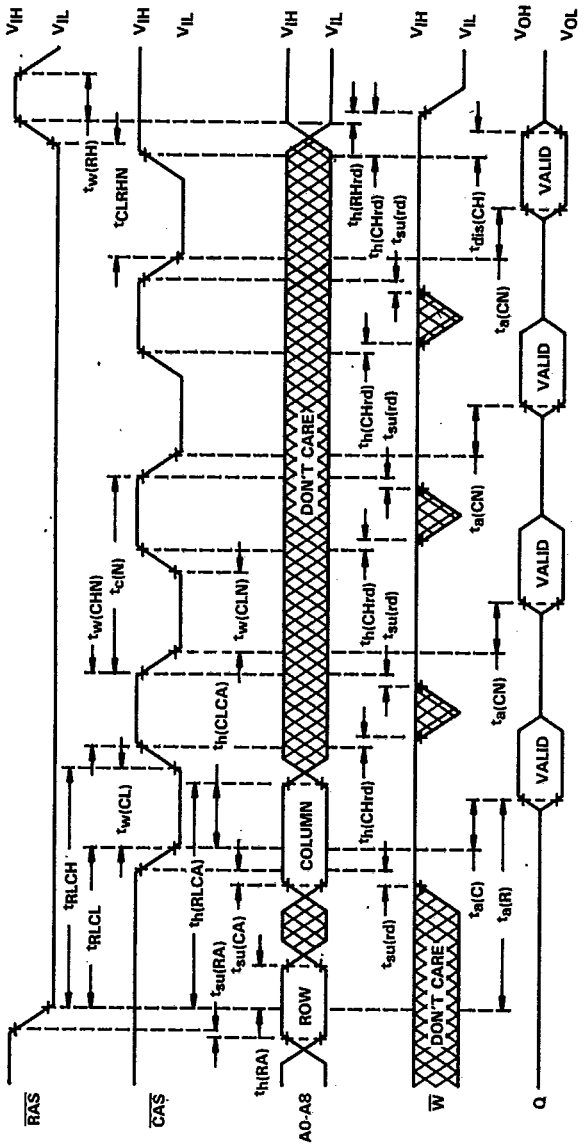
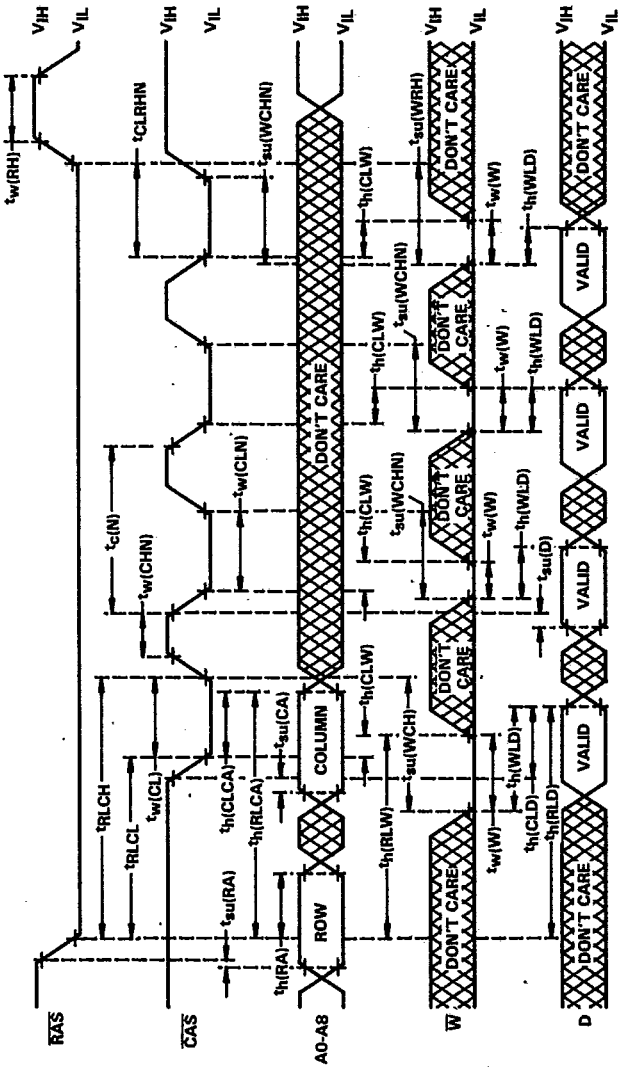
nibble-mode read cycle timing



nibble-mode write cycle timing



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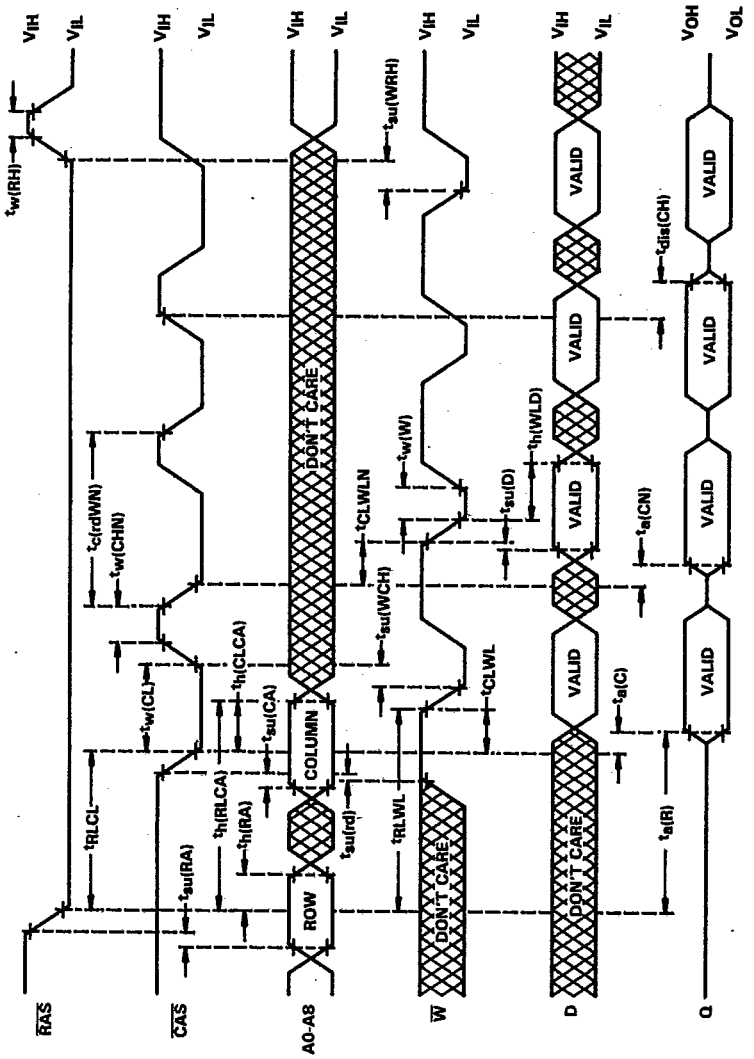
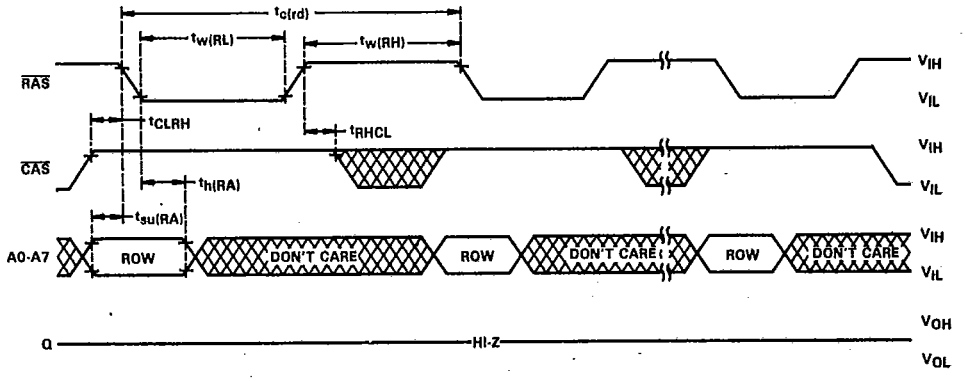
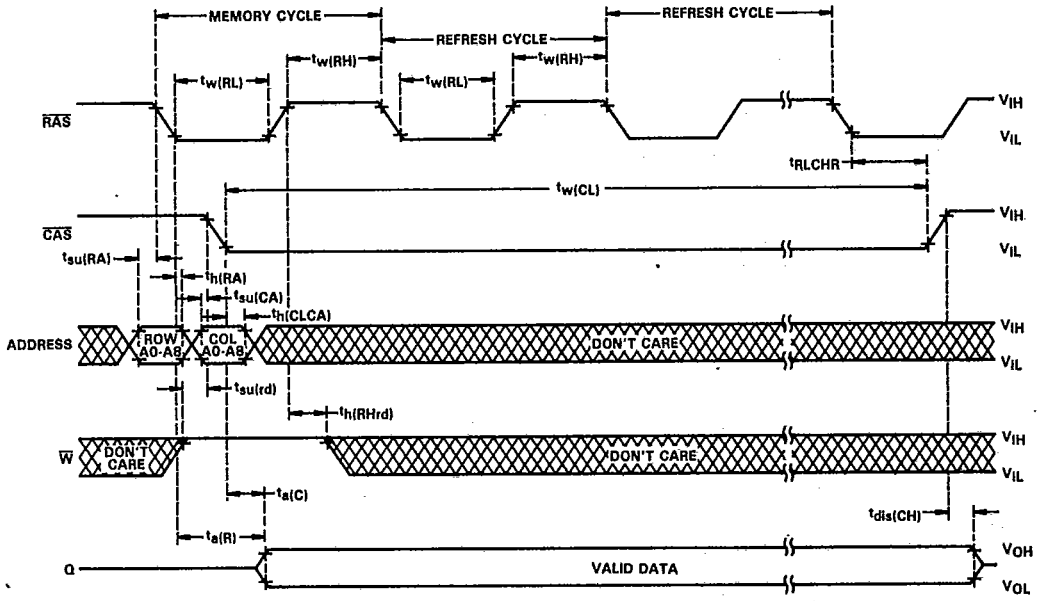
nibble-mode read-modify-write-cycle timing



$\overline{RAS}$-only refresh cycle timing



hidden refresh cycle timing



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automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing